

ENGINEERING MEMO

Initiated by:		Andrew Williams	Andrew Williams		
Project Manager:		Tom Booler	Tom Booler		
Proposed Pr	riority:	Fast Track	Normal		
Title: BFIF BL233 crashes, power cycle fixes it					
Affected item(s):					
A small number of the 56 deployed BFIF boxes at the MRO on long baseline tiles.					
Technical description of problem:					
Control of four occasions, three long baseline files at the MRO have seen a complete loss of communication between the Raspberry Pi on the BFIF board and the BL233 chip (a custom PIC microcontroller) on the SPIU. Tiles LBC7 and LBD3 failed at the same instant on November 15 th , 2017. Tiles LBE2 and LBC7 (again) failed at the same instant on Feb 6 th , 2018. In all cases (four failures on three tiles), the symptoms were the same – no communication on the serial port to the BL233 chip. In one of those four failures (LBC7 on Nov 15 th), the fault disappeared after power to the BFIF/SPIU was removed and restored, rebooting the BL233. Tile LBD3 had the boards serviced before a power cycle was attempted. For now, we are assuming that LBE2 and LBC7 can be fixed by a simple power cycle.					
Reason for change and expected benefits:					
The goal is to either prevent the BL233 from crashing (by reproducing the problem in the lab and changing the circuit), or to modify the system to be able to power cycle the BL233 chip if necessary using a GPIO output from the Raspberry Pi.					
Effective Date:					
Reason for given effective date:					
Expected impact on cost (\$AUD):					
Impact on Minin schedule:		Vinimal, faults seem to o	imal, faults seem to occur rarely, during lightning storms.		
Other impacts:					
Attached Document(s):					
Author: Andrew Williams		/illiams	Signature:		
Email: Andrew.Williams@		/illiams@curtin.ed.au	Date:		